PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Form PCT/IPEA/416
SP 23898 PM		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/EP2004/052548	14.10.2004	14.10.2003
International Patent Classification (IPC) or national classification and IPC		
H01L21/762, H01L21/304		
Applicant		
TRACIT TECHNOLOGIES et al.		

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 7 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
   a. ☒ *sent to the applicant and to the International Bureau)* a total of 7 sheets, as follows:
      ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
      ☒ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
   b. ☐ *(sent to the International Bureau only)* a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains indications relating to the following items:

☒	Box No. I	Basis of the opinion
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☒	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☒	Box No. VIII	Certain observations on the international application

Date of submission of the demand	Date of completion of this report
11.08.2005	11.01.2006
Name and mailing address of the international preliminary examining authority:	Authorized Officer
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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/EP2004/052548

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.

   ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
   - ☐ international search (under Rules 12.3 and 23.1(b))
   - ☐ publication of the international application (under Rule 12.4)
   - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)

2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages	
1-20	as originally filed
Claims, Numbers	
1-35	received on 16.08.2005 with letter of 11.08.2005
Drawings, Sheets	
1/6-6/6	as originally filed

   ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing

3. ☐ The amendments have resulted in the cancellation of:
   - ☐ the description, pages
   - ☐ the claims, Nos.
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

4. ☒ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
   - ☐ the description, pages
   - ☒ the claims, Nos. 3,4
   - ☐ the drawings, sheets/figs
   - ☐ the sequence listing *(specify)*:
   - ☐ any table(s) related to sequence listing *(specify)*:

* *If item 4 applies, some or all of these sheets may be marked "superseded."*

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

International application No.
PCT/EP2004/052548

Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	5,8,25,35-37
	No:	Claims	1,2,6,7,9-24,26-34
Inventive step (IS)	Yes:	Claims	
	No:	Claims	1,2,5-37
Industrial applicability (IA)	Yes:	Claims	1,2,5-37
	No:	Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VI Certain documents cited

1. Certain published documents (Rule 70.10)

and / or

2. Non-written disclosures (Rule 70.9)

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item I

Basis of the report

The amendments filed with the letter dated 11.08.2005 introduce subject-matter which extends beyond the content of the application as filed, contrary to Article 34(2)(b) PCT. Indeed, the combination of the newly filed claims 1 and 3 - i.e, the fact that the protective layer is removed locally before the routing stage of the first wafer and is then eliminated after the routing stage routing - is not supported by the originally filed application. It should be noted that the originally filed application only discloses either a protective layer which is eliminated after the routing stage but not removed locally before the routing stage (see figure 10: the protective layer is eliminated during the routing stage; see also former claim 23 which is dependent on claim 22, but not on claim 25), or a protective layer which is removed locally before the routing stage but not eliminated after the routine stage (see figure 7). Therefore, the claimed invention in respect of claim 3 and its dependent claim 4 is not be examined.

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:
   - D1: EP-A-1 059 663 (CANON KABUSHIKI KAISHA) 13 December 2000 (2000-12-13)
   - D2: EP-A-1 026 728 (CANON KABUSHIKI KAISHA) 09 August 2000 (2000-08-09)
   - D3: PATENT ABSTRACTS OF JAPAN vol. 2000, no. 09, 13 October 2000 (2000-10-13) -& JP 2000 173961 A (SHARP CORP), 23 June 2000 (2000-06-23)
   - D4: EP-A-1 189 266 (SHINETSU HANDOTAI KK) 20 March 2002 (2002-03-20)

2. The present application does not meet the criteria of Article 33(1) PCT, because the subject-matter of the newly filed independent claims 1 and 9 is not new in the sense of Article 33(2) PCT.

2.1 Referring to independent claim 1, document D1 discloses a method for assembling a

first and a second wafer (see abstract), of which at least the first, known as chamfered wafer, has at least a chamfered edge (see page 5, paragraphs 23 and 24; figures 3A and 3B), comprising:

- covering the first wafer with a protective layer (see page 5, lines 55 and 58: the substrate is masked and the mask is then removed after the etching step. It is therefore considered that this mask pattern that covers the substrate plays the role of the protective layer);
- a routing stage of at least one part of the chamfered edge of the first wafer (see page 5, paragraph 25; figure 1D);
- eliminating the protective layer after routing of the first wafer (see page 5, line 58);
- then, an assembling stage of the first wafer, routed, and of the second wafer (see page 5, paragraph 25; figure 1E).

Therefore, the subject-matter of independent **claim 1** is not new (Art. 33(2) PCT).

For the sake of completeness, independent claim 1 is also not new over the disclosure of document D2 (see column 19, paragraphs 141 and 143: it is considered that the resin layer is the claimed protective layer; column 20, paragraphs 146 and 147; figures 4C and 5E).

2.2 Referring to independent claim 9, document D1 discloses a method for transplanting a layer of material or circuits or components (see abstract), known as transplant layer, comprising:

- the routing of a first wafer of material, in which the transplant layer is made, at least around or on the periphery of this transplant layer (see page 5, paragraph 25; figure 1D), over a thickness ed less than the thickness e of the first wafer, but greater than a thickness of the transplant layer (see page 5, line 28; figure 1D);
- the transplanting of this layer onto a second wafer of material (see page 5, paragraph 25; figures 1E-1G).

Hence, document D1 discloses all the technical features of independent claim 3. Therefore, the subject-matter of independent **claim 9** is not new (Art. 33(2) PCT).

For the sake of completeness, independent claim 1 is also not new over the disclosure of

document D3 (see abstract; page 7, paragraph 47; figures 2-4).

3. Dependent claims 2, 5-8, 10-37 do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty and/or inventive step (Article 33(2) and (3) PCT), see documents D1-D4 and the corresponding passages in the search report.

4. All claims 1,2,5-37 fulfill the requirements of Article 33(4) PCT concerning the industrial applicability.

Re Item VI
Certain documents cited

Certain published documents

Application No Patent No	Publication date *(day/month/year)*	Filing date *(day/month/year)*	Priority date *(valid claim)* *(day/month/year)*
WO2004008525	22/01/2004	16/07/2003	17/07/2002
WO2004081974	23/09/2004	12/03/2004	14/03/2003

Re Item VIII
Certain observations on the international application

The application does not meet the requirements of Article 6 PCT because independent claims 1 and 9 are not clear, for the following reasons:

- in said both claims, the terms "routing", "transplanting" and "assembling" have no well-recognised meaning, thereby rendering the definition of the subject-matter of said claims unclear. It should be noted that these terms have been considered respectively as "trimming", "transferring" and "bonding".

- moreover, both claims do not meet the requirement following from Article 6 PCT taken in combination with Rule 6.3(b) since they do not contain all the technical features essential to the definition of the invention.

Firstly, the disclosed routing stage does not enable the skilled person to determine which technical features are necessary to perform the invention. Indeed, the disclosure of this step is too vague, as there are many ways to perform this trimming. For example, the etching step described in document D4 (see column 6, paragraphs 34-37; figures 1c and 1d) corresponds to a trimming process.

Secondly, it is clear from the description of the present application that the face of the first wafer which comes into contact with the second wafer during the bonding is the one from which the trimming is performed. This essential feature is missing from claims 1 and 3.

- in claim 9, the fact that the order of the process steps is not given does not comply with the requirements of Article 6 PCT. Indeed, it is clear from the description of the present application that the trimming step has to be performed before the bonding step (see page 5, lines 1-7).

CLAIMS

1. Method for assembling a first and a second wafer (12, 14, 22, 24), of which at least the first, known as chamfered wafer, has at least a chamfered edge (7, 17), comprising:

- covering the first wafer with a protective layer (18),
- a routing stage of at least one part of the chamfered edge of the first wafer (12, 22);
- eliminating the protective layer (18) after routing of the first wafer,
- then, an assembling stage of the first wafer, routed, and of the second wafer.

2. Method as in claim 1, further comprising, after assembling, a thinning out stage of at least the first wafer, leaving at least a layer (16) on the second wafer.

3. Method as in claim 1 or 2, the protective layer being eliminated locally, before routing of the first wafer, in a zone located above the zone to be routed of the first wafer.

4. Method as in the previous claim, the local elimination of the protective layer being performed via lithography and etching.

5. Method as in one of claims 1 to 4, the routing stage being performed over the entire thickness e of the first wafer.

6. Method as in one of claims 1 to 4, the routing stage being performed over a thickness ed less than the thickness e of the first wafer.

7. Method as in claim 6, the routing stage being performed over a thickness ed greater than or equal to a thickness of a layer (16, 28) of the first wafer to be transplanted onto the second wafer.

8. Method as in claim 6, the routing stage being performed over a thickness ed less or equal to a thickness of a layer (16, 28) of the first wafer to be transplanted or transferred onto the second wafer.

9. Method for transplanting a layer (16, 28) of material or circuits or components, known as transplant layer, comprising:

- the routing of a first wafer (12, 22) of material, in which the transplant layer is made, at least around or on the periphery of this transplant layer, over a thickness ed less than the thickness e of the first wafer, but greater than a thickness of said transplant layer (16, 28);
- the transplanting of this layer onto a second wafer (14, 24) of material.

10. Method as in claim 9, the first wafer previously being covered with a protective layer (18).

11. Method as in claim 10, the protective layer being eliminated locally, before routing of the first wafer, in a zone located above the zone to be routed of the first wafer.

12. Method as in claim 11, the local elimination of the protective layer being performed via lithography and etching.

13. Method as in claim 10, the protective layer (18) being eliminated after routing of the first wafer.

14. Method as in any of claims 5 to 13, in which a part of the material of the transplant layer is eliminated during routing.

15. Method as in one of claims 9 to 14, the fist wafer being chamfered and comprising at least a chamfered edge (5).

16. Method as in any of claims 1 to 8 or 15, the routing stage being performed over a width Ld, measured on a plane parallel to that of the first wafer, at least equal to the width L of the chamfered edge, measured on the same plane.

17. Method as in one of claims 1 to 16, comprising an additional routing stage after assembling the first and second wafers.

18. Method as in one of claims 1 to 17, the routing stage being performed over a thickness ed of the first wafer of between 1 µm and 100 µm.

19. Method as in any of claims 1 to 18, the routing stage being performed over a width Ld, measured on a plane parallel to that of the first wafer, at least equal to the width of the zone of this first wafer which can not, without routing, be assembled with the second wafer.

20. Method as in any of claims 1 to 19, the routing stage being performed over a width Ld, measured on a plane parallel to that of the first wafer of between 100 µm and 5 mm.

21. Method as in any of the previous claims, the first wafer having a weakened plane (26) defining a thin layer in the wafer.

22. Method as in the previous claim, the first wafer being routed over a thickness greater than that of the thin layer.

23. Method as in claim 22, followed by:

- a thinning out stage via separation of the first wafer along the weakened plane, so as to leave

the thin layer on the second wafer and leave a free portion (23) of the first substrate;

- a new creating stage of a new weakened plane in the portion (23) that remained free of the first substrate;
- an assembling stage of this portion (23) with a third substrate.

24. Method as in any of claims 21 to 23, the embrittlement plane being performed via ion implantation or via the creating of a buried porous zone or via the creating of a removable bonding interface.

25. Method as in any of claims 1 to 24, the first wafer comprising a lateral shoulder (25), eliminated during the routing stage.

26. Method as in any of claims 1 to 25, the assembling of the two substrates being performed via molecular adhesion or via bonding using an adhesive substance.

27. Method as in any of the previous claims, components or circuits (16) having been made in the first wafer before routing.

28. Method as in any of the previous claims, the routing taking place after a previous surface preparation stage of the first wafer with the purpose of assembling or transplanting.

29. Method as in any of claims 1 to 27, the routing taking place before a previous surface preparation stage of the first wafer with the purpose of assembling or transplanting.

30. Method as in any of the previous claims, the routing being performed via mechanical or chemical or mechano-chemical etching or polishing or via plasma etching or via a combination of at least two of these types of etching.

31. Method as in any of the previous claims, at least one of the two wafers being made in a semiconductor material.

32. Method as in the previous claim, at least one of the two wafers being made in silicon or in a III-V type semiconductor material.

33. Method as in any of claims 1 to 31, at least one of the two wafers being made in Germanium or in Germanium silicide (SiGe) or in a piezoelectric material or in an insulating material.

34. Method as in any of the previous claims, the routing stage being performed in a regular manner around the first wafer.

35. Method as in any of claims 1 to 33, the routing stage being performed in an irregular manner around the first wafer, creating a plane (44).

36. Method as in any of claims 1 to 33 or 35, the routing stage being performed in an irregular manner, creating a marking zone (50 and 51).

37. Method as in claim 36, further comprising a marking stage of the first wafer.